CLAIMS

1. A conditional vector arithmetic method comprising:

an arithmetic decision step of, when an arithmetic processing target data is obtained in an arithmetic processing step of executing an arithmetic processing, computing and deciding in parallel therewith whether the arithmetic is to be executed or not; and

an arithmetic control step of, when an arithmetic control is exerted to execute vector arithmetic in the arithmetic processing step, exerting the arithmetic control so as to execute the arithmetic for the arithmetic processing target data and output a result of the arithmetic or output the target data without executing the arithmetic, according to a decided result in the arithmetic decision step,

said conditional vector arithmetic method enabling conditional arithmetic to be processed by vector arithmetic.

2. A conditional vector arithmetic method comprising

a pipeline processing including:

a first stage having a source data supply processing step of starting supply of data in accordance with issue of a vector arithmetic instruction, and a state flag retain processing step which is executed in parallel with said step, of sequentially retaining a state of a data which is supplied to a prescribed

source among the data which are supplied in the source data supply processing, and outputting the state as a state flag;

a second stage having an arithmetic processing step of performing arithmetic using the data which are supplied in the source data supply processing step and outputting an arithmetic result, and a condition decision processing step which is executed in parallel with said step, of making a condition decision of the state flag with a condition which is issued in accordance with the vector arithmetic instruction, and providing information as to whether the condition is satisfied or not to a control processing step; and

a third stage having an arithmetic result storage processing step of successively storing the arithmetic results which are obtained in the arithmetic processing step, to exert a control for executing a vector arithmetic processing by executing the pipeline processing, and

the control processing step of exerting a control so as to execute the arithmetic processing when the information which is output in the condition decision processing indicates that the condition is satisfied, and output the data which is supplied to the prescribed source among the data which are supplied in the source data supply processing step as it is as the arithmetic result of the arithmetic processing when the information indicates that the condition is not satisfied.

3. A conditional vector arithmetic unit comprising:

an arithmetic means for executing an arithmetic processing;

an arithmetic decision means for, when the arithmetic means obtains an arithmetic processing target data, computing and deciding in parallel therewith whether the arithmetic is to be executed or not; and

an arithmetic control means for, when the arithmetic means exerts an arithmetic control to execute vector arithmetic, exerting an arithmetic control so as to execute the arithmetic for the arithmetic processing target data and output a result of the arithmetic or output the data without executing the arithmetic, according to a decided result of the arithmetic decision means,

said conditional arithmetic unit enabling the conditional arithmetic to be processed by the vector arithmetic.

4. A conditional vector arithmetic unit comprising:

a source data supply means for starting supply of first to N-th source data (N is an integer which is equal to or larger than 2) in accordance with issue of a vector arithmetic instruction;

first to N-th registers for temporarily retaining the first to N-th source data which are supplied from the source

data supply means;

an arithmetic means for performing arithmetic using outputs of the first to N-th registers;

a pipeline register for temporarily retaining an arithmetic result which is output by the arithmetic means;

an arithmetic result storage means for successively storing outputs of the pipeline register;

a state flag retain means for sequentially retaining state flag information which indicates a property of a predetermined source data among the first to N-th source data;

a condition decision means for outputting information which indicates whether a condition of the vector arithmetic instruction is satisfied or not, on the basis of an output of the state flag retain means and condition information which is specified by the vector arithmetic instruction; and

a control means for generating a control signal for executing the vector arithmetic instruction by a pipeline processing comprising a first stage in which the source data supply means supplies the source data and stores the data in the first to N-th registers and, in parallel therewith, the state flag retain means retains the state flag information and outputs the same, a second stage in which the arithmetic means outputs arithmetic processing results of the outputs of the first to N-th registers to the pipeline register and, in parallel therewith, the condition decision means outputs the

information indicating whether the condition of the vector arithmetic instruction is satisfied or not, and a third stage in which the outputs of the pipeline register are stored in the arithmetic result storage means, and

generating a mode selection signal for, upon receipt of the information which is output by the condition decision means, outputting a value of the prescribed source data among the first to N-th source data as it is as the output of the arithmetic means when the condition is not satisfied, and selecting the arithmetic result of the arithmetic means to output the same when the condition is satisfied.